

### FEATURES

- High slew rate: 9 V/μs**
- Wide bandwidth: 4 MHz**
- Low supply current: 250 μA/amplifier maximum**
- Low offset voltage: 3 mV maximum**
- Low bias current: 100 pA maximum**
- Fast settling time**
- Common-mode range includes V+**
- Unity-gain stable**

### APPLICATIONS

- Active filters**
- Fast amplifiers**
- Integrators**
- Supply current monitoring**

### GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/μs with a supply current under 250 μA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

With a wide output swing, within 1.5 V of each supply, low power consumption, and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. The OP282 is available in the standard 8-lead narrow SOIC and MSOP packages. The OP482 is available in PDIP and narrow SOIC packages.

### PIN CONNECTIONS

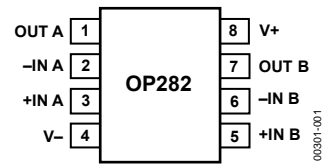


Figure 1. 8-Lead Narrow-Body SOIC (S-Suffix) [R-8]

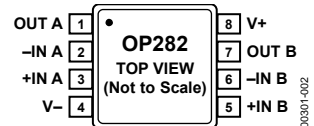


Figure 2. 8-Lead MSOP [RM-8]

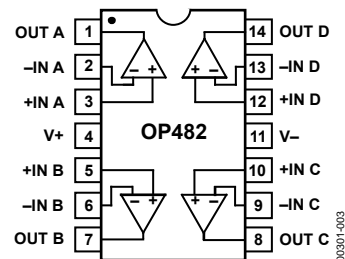


Figure 3. 14-Lead PDIP (P-Suffix) [N-14]

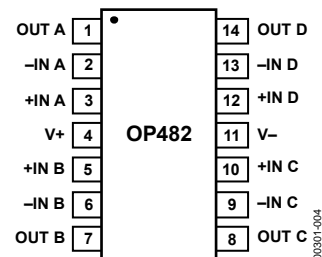


Figure 4. 14-Lead Narrow-Body SOIC (S-Suffix) [R-14]

### Rev. G

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## TABLE OF CONTENTS

Features .....	1
Applications .....	1
General Description .....	1
Pin Connections .....	1
Revision History .....	2
Specifications .....	3
Electrical Characteristics .....	3
Absolute Maximum Ratings .....	4
Thermal Resistance .....	4

ESD Caution .....	4
Typical Performance Characteristics .....	5
Applications Information .....	12
High-Side Signal Conditioning .....	12
Phase Inversion .....	12
Active Filters .....	12
Programmable State Variable Filter .....	13
Outline Dimensions .....	14
Ordering Guide .....	16

## REVISION HISTORY

### 7/08—Rev. F to Rev. G

Changes to Phase Inversion Section .....	12
Deleted Figure 45 .....	12
Added Figure 45 and Figure 46 .....	12
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	16

### 10/04—Rev. E to Rev. F

Deleted 8-Lead PDIP .....	Universal
Added 8-Lead MSOP .....	Universal
Changes to Format and Layout .....	Universal
Changes to Features .....	1
Changes to Pin Configurations .....	1
Changes to General Description .....	1
Changes to Specifications .....	3
Changes to Absolute Maximum Ratings .....	4
Changes to Table 3 .....	4
Added Figure 5 through Figure 20; Renumbered Successive Figures .....	5
Updated Figure 21 and Figure 22 .....	7
Updated Figure 23 and Figure 27 .....	8
Updated Figure 29 .....	9
Updated Figure 35 and Figure 36 .....	10
Updated Figure 43 .....	11
Changes to Applications Information .....	12
Changes to Figure 44 .....	12
Deleted OP282/OP482 Spice Macro Model Section .....	9
Deleted Figure 4 .....	9
Deleted OP282 Spice Marco Model .....	10
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	14

### 10/02—Rev. D to Rev. E

Edits to 8-Lead Epoxy DIP (P-Suffix) Pin .....	1
Edits to Ordering Guide .....	3
Edits to Outline Dimensions .....	11

### 9/02—Rev. C to Rev. D

Edits to 14-Lead SOIC (S-Suffix) Pin .....	1
Replaced 8-Lead SOIC (S-Suffix) .....	11

### 4/02—Rev. B to Rev. C

Wafer Test Limits Deleted .....	2
Edits to Absolute Maximum Ratings .....	3
Dice Characteristics Deleted .....	3
Edits to Ordering Guide .....	3
Edits to Figure 1 .....	7
Edits to Figure 3 .....	8
20-Position Chip Carrier (RC Suffix) Deleted .....	11

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

At  $V_s = \pm 15.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted; applies to both A and G grades.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	OP282		0.2	3	mV
		OP282, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			4.5	mV
Input Bias Current	$I_B$	OP482		0.2	4	mV
		OP482, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			6	mV
Input Offset Current	$I_{OS}$	$V_{CM} = 0\text{ V}$		3	100	pA
		$V_{CM} = 0\text{ V}^1$			500	pA
Input Voltage Range	CMRR	$V_{CM} = 0\text{ V}$		1	50	pA
		$V_{CM} = 0\text{ V}^1$			250	pA
Common-Mode Rejection Ratio		$-11\text{ V} \leq V_{CM} \leq +15\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-11		+15	V
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$	70	90		dB
		$R_L = 10\text{ k}\Omega$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			8		$\text{pA}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$	13.5	13.9		V
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$		-13.9	-13.5	V
Short-Circuit Limit	$I_{SC}$	Source	3	10		mA
		Sink		-12	-8	mA
Open-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$		200		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_s = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25	316	$\mu\text{V}/\text{V}$
Supply Current/Amplifier	$I_{SY}$	$V_o = 0\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		210	250	$\mu\text{A}$
Supply Voltage Range	$V_s$		$\pm 4.5$		$\pm 18$	V
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$	7	9		$\text{V}/\mu\text{s}$
Full-Power Bandwidth	$BW_P$	1% distortion		125		kHz
Settling Time	$t_s$	To 0.01%		1.6		$\mu\text{s}$
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$\phi_M$			55		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		1.3		$\mu\text{V}$ p-p
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		36		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$			0.01		$\text{pA}/\sqrt{\text{Hz}}$

<sup>1</sup> The input bias and offset currents are characterized at  $T_A = T_J = 85^\circ\text{C}$ . Bias and offset currents are guaranteed but not tested at  $-40^\circ\text{C}$ .

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameters	Ratings
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage <sup>1</sup>	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Operating Temperature Range OP282G, OP282A, OP482G	−40°C to +85°C
Junction Temperature Range P-Suffix (N), S-Suffix (R), RM Packages	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

<sup>1</sup> For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device in socket for CERDIP and PDIP.  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC\_N or MSOP packages.

Table 3.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead MSOP [RM]	206	44	°C/W
8-Lead SOIC_N (S-Suffix) [R]	157	56	°C/W
14-Lead PDIP (P-Suffix) [N]	83	39	°C/W
14-Lead SOIC_N (S-Suffix) [R]	104	36	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

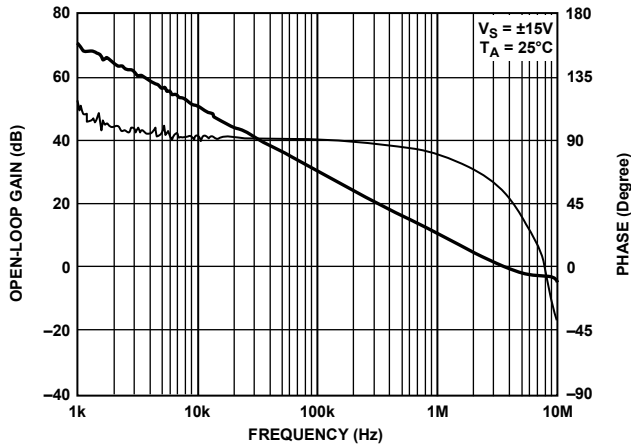


Figure 5. OP282 Open-Loop Gain and Phase vs. Frequency

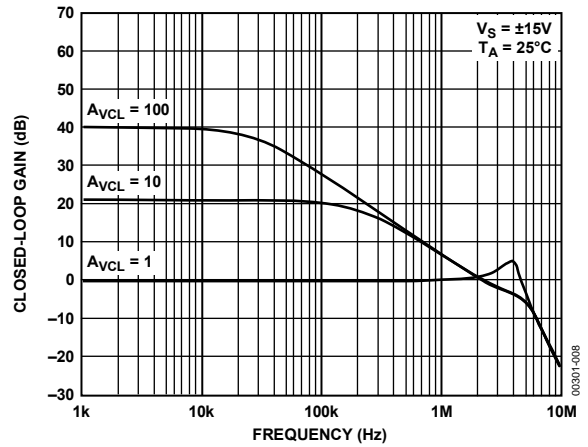


Figure 8. OP282 Closed-Loop Gain vs. Frequency

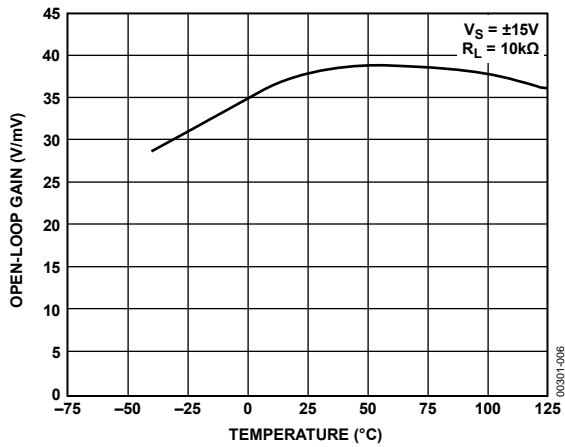


Figure 6. OP282 Open-Loop Gain vs. Temperature

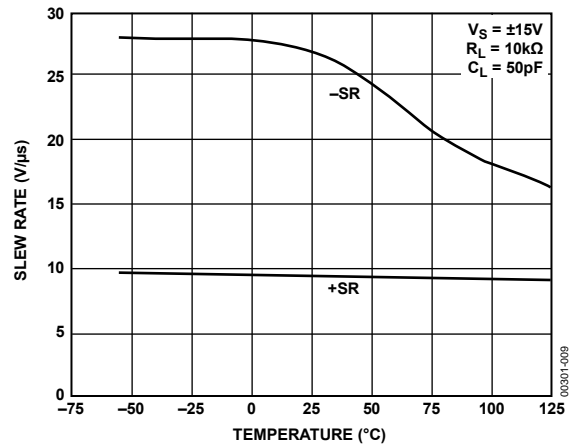


Figure 9. OP282 Slew Rate vs. Temperature

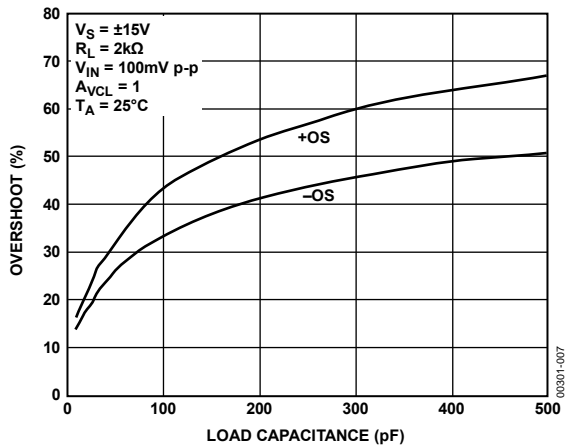


Figure 7. OP282 Small Signal Overshoot vs. Load Capacitance

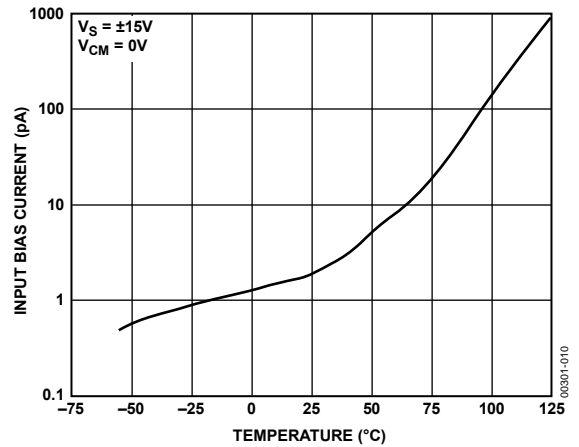


Figure 10. OP282 Input Bias Current vs. Temperature

# OP282/OP482

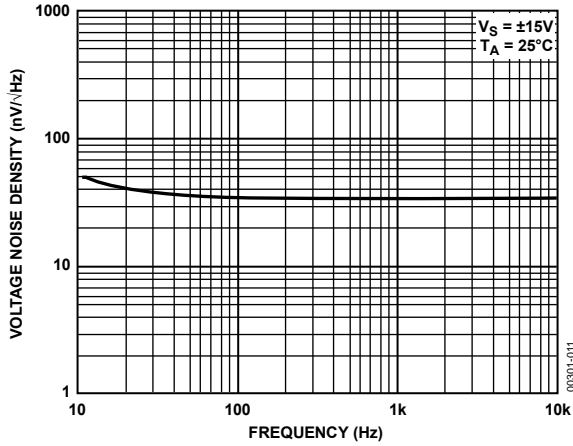


Figure 11. OP282 Voltage Noise Density vs. Frequency

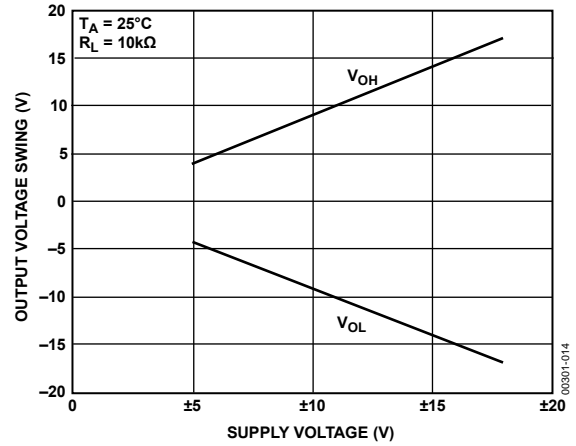


Figure 14. OP282 Output Voltage Swing vs. Supply Voltage

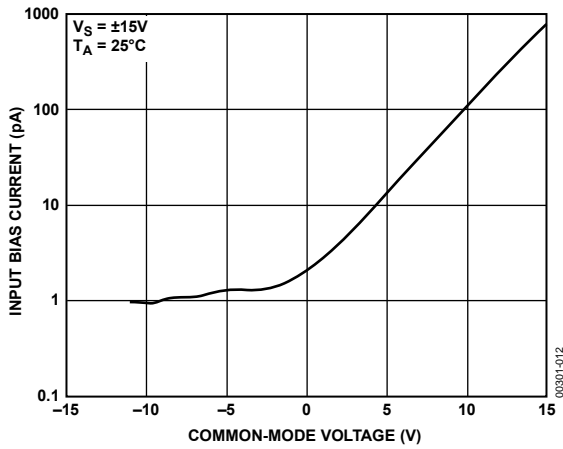


Figure 12. OP282 Input Bias Current vs. Common-Mode Voltage

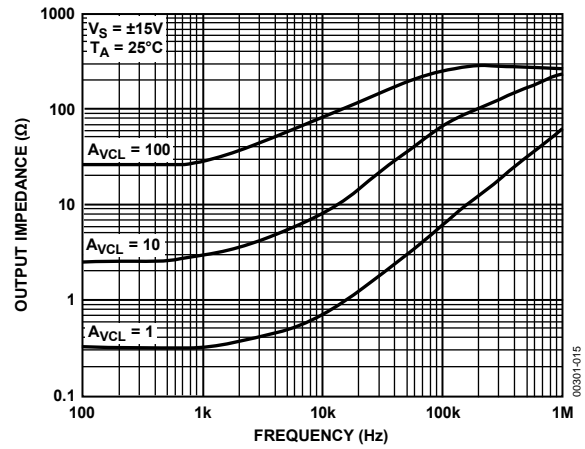


Figure 15. OP282 Closed-Loop Output Impedance vs. Frequency

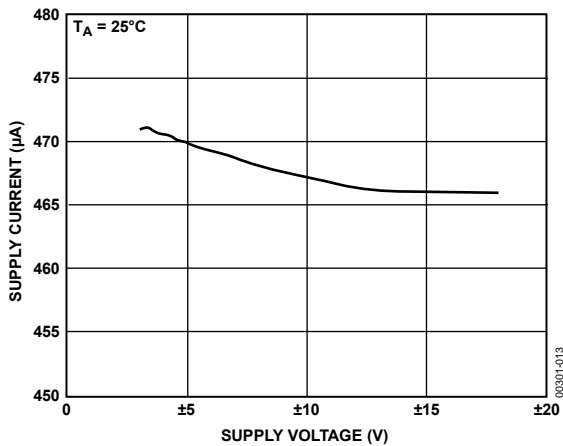


Figure 13. OP282 Supply Current vs. Supply Voltage

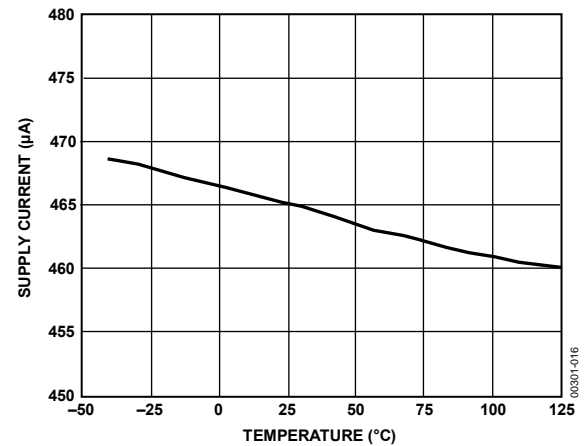


Figure 16. OP282 Supply Current vs. Temperature

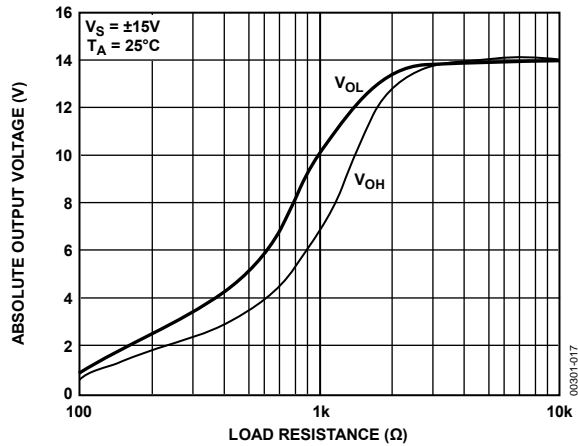


Figure 17. OP282 Absolute Output Voltage vs. Load Resistance

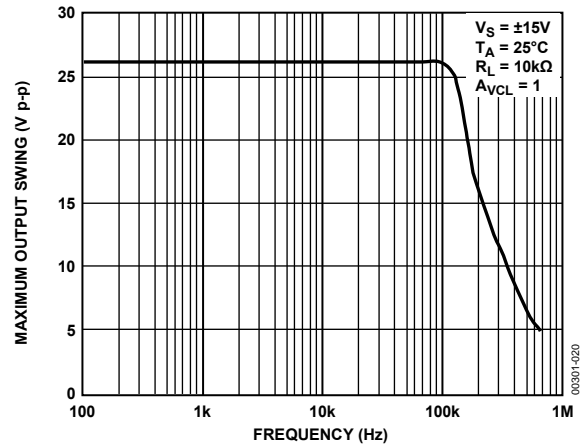


Figure 20. OP282 Maximum Output Swing vs. Frequency

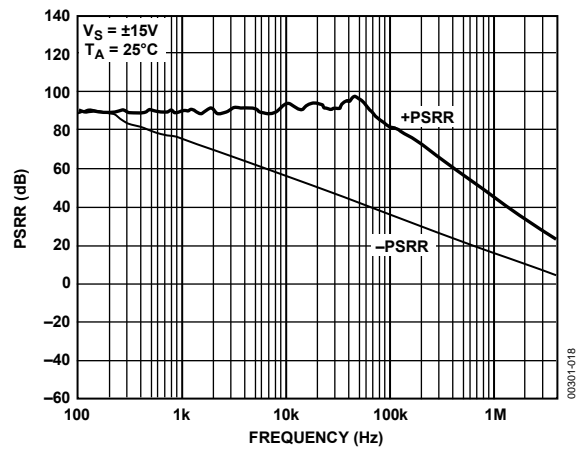


Figure 18. OP282 PSRR vs. Frequency

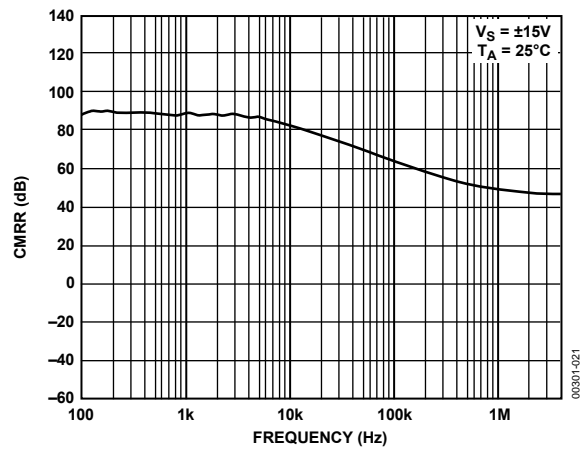


Figure 21. OP282 CMRR vs. Frequency

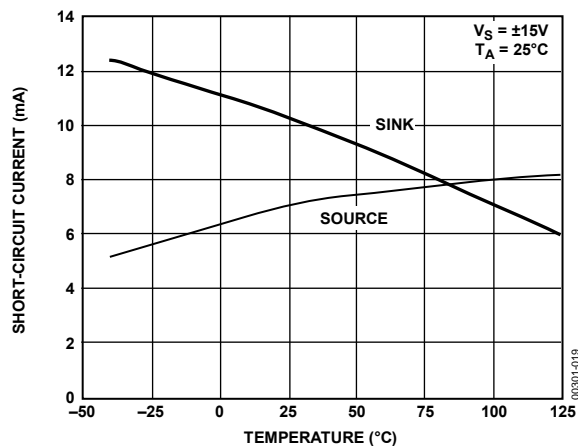


Figure 19. OP282 Short-Circuit Current vs. Temperature

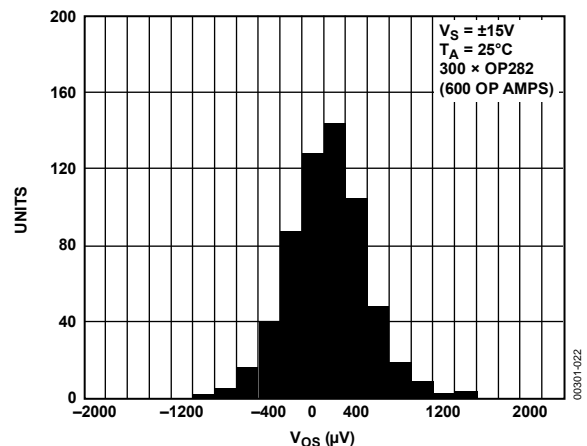


Figure 22. OP282  $V_{OS}$  Distribution SOIC\_N Package

# OP282/OP482

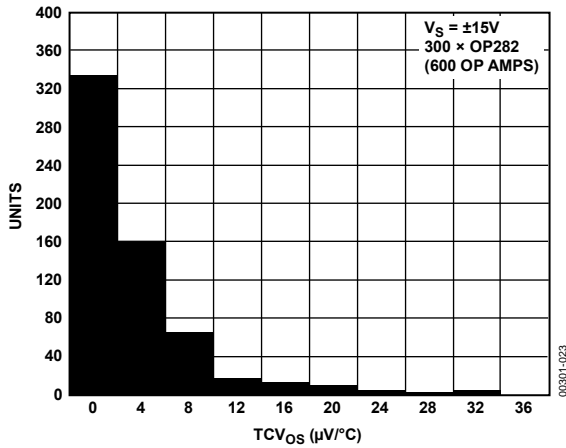


Figure 23. OP282 TCVOs Distribution SOIC\_N Package

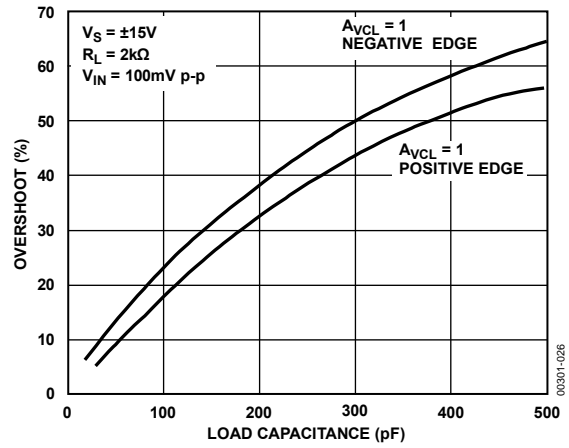


Figure 26. OP482 Small Signal Overshoot vs. Load Capacitance

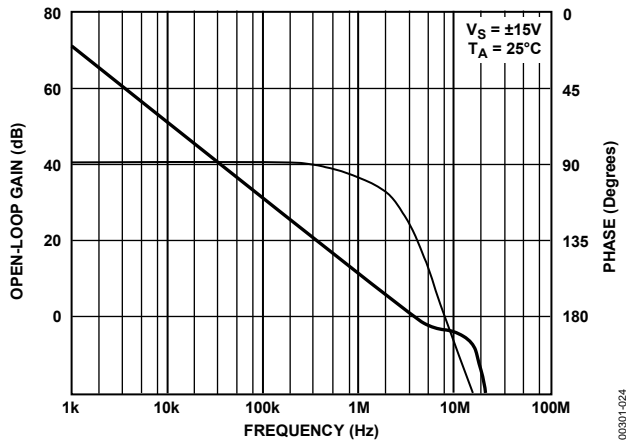


Figure 24. OP482 Open-Loop Gain, Phase vs. Frequency

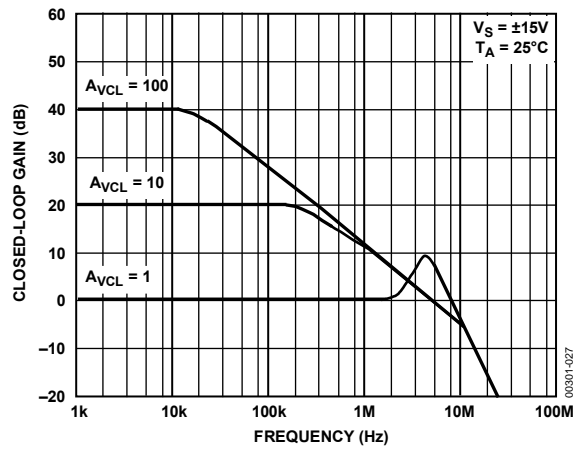


Figure 27. OP482 Closed-Loop Gain vs. Frequency

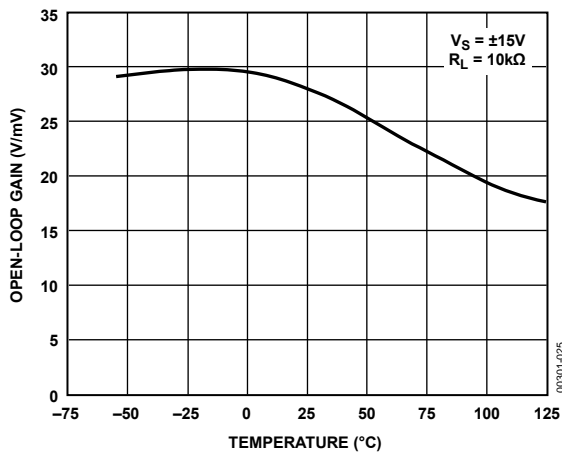


Figure 25. OP482 Open-Loop Gain (V/mV)

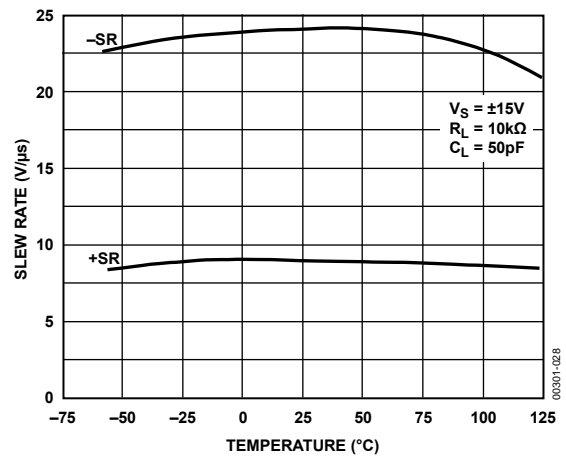


Figure 28. OP482 Slew Rate vs. Temperature



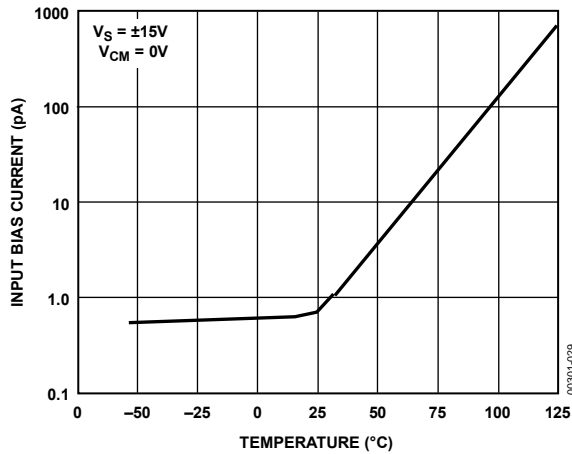


Figure 29. OP482 Input Bias Current vs. Temperature

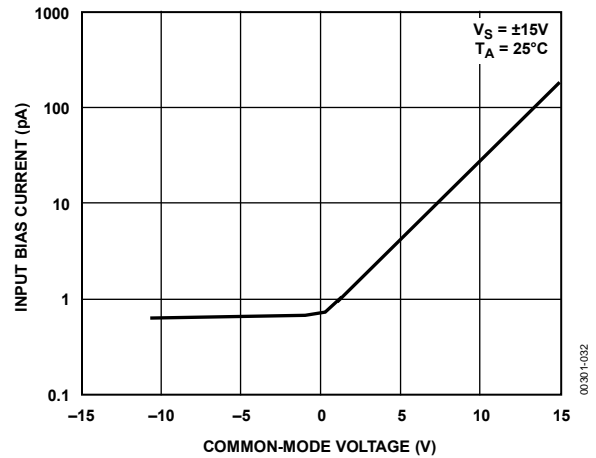


Figure 32. OP482 Input Bias Current vs. Common-Mode Voltage

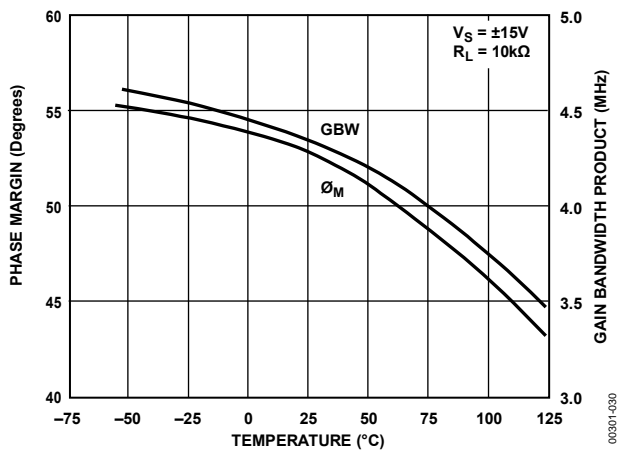


Figure 30. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature

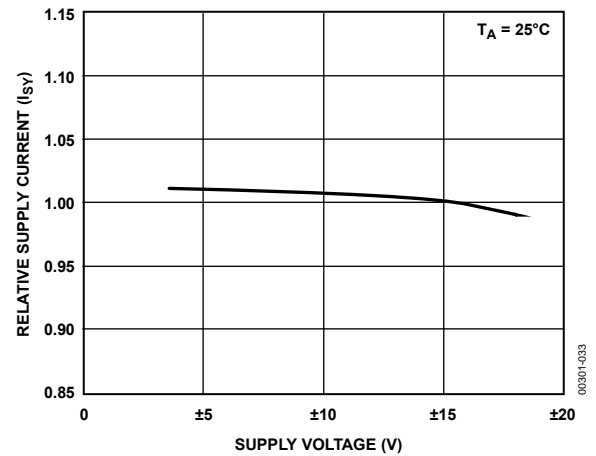


Figure 33. OP482 Relative Supply Current vs. Supply Voltage

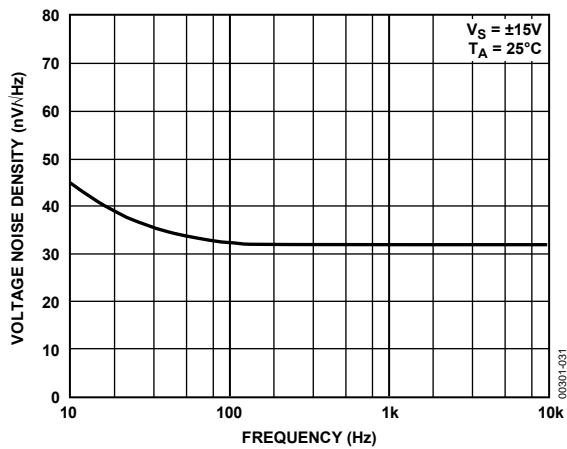


Figure 31. OP482 Voltage Noise Density vs. Frequency

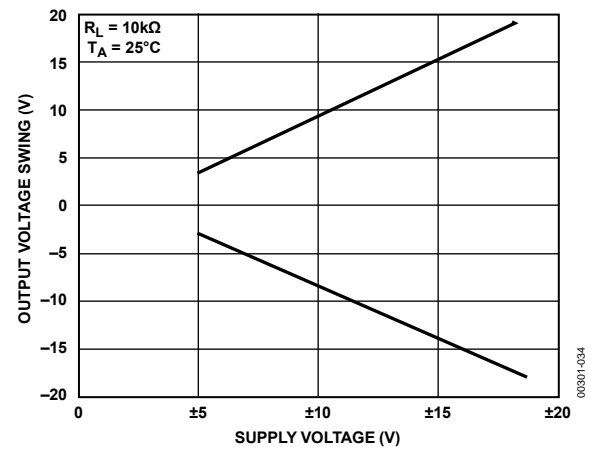


Figure 34. OP482 Output Voltage Swing vs. Supply Voltage

# OP282/OP482

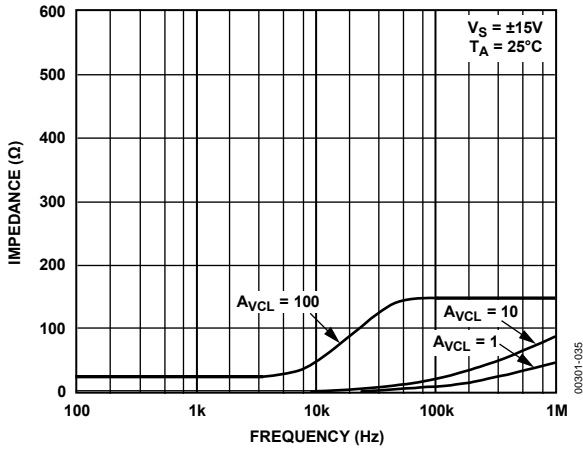


Figure 35. OP482 Closed-Loop Output Impedance vs. Frequency

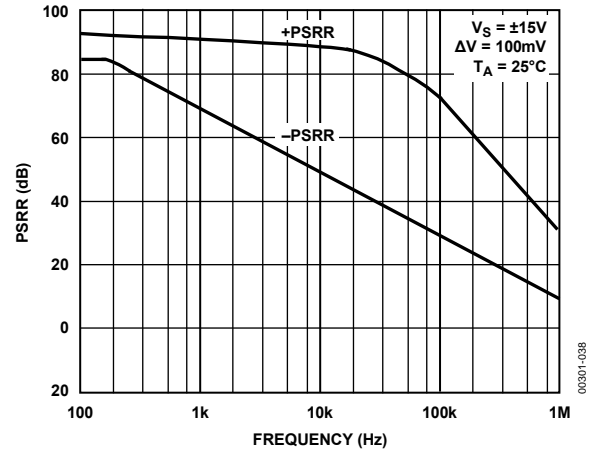


Figure 38. OP482 Power Supply Rejection Ratio (PSRR) vs. Frequency

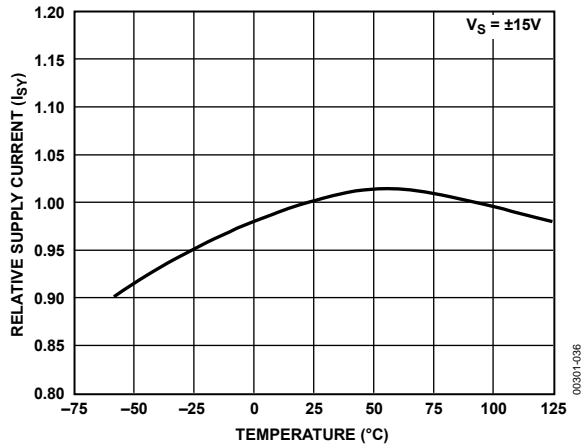


Figure 36. OP482 Relative Supply Current vs. Temperature

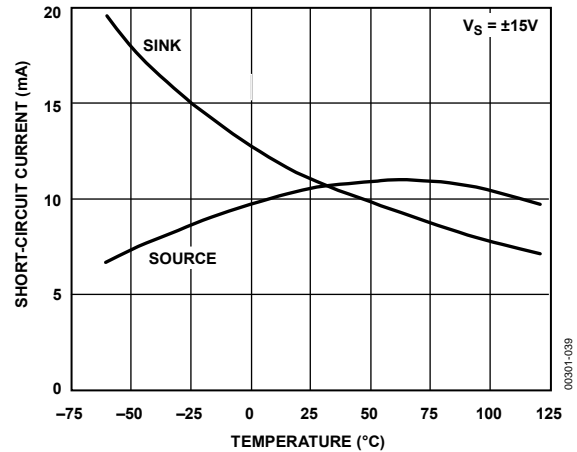


Figure 39. OP482 Short-Circuit Current vs. Temperature

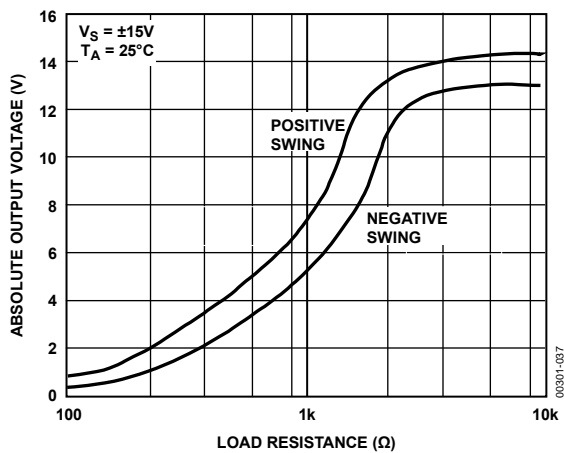


Figure 37. OP482 Maximum Output Voltage vs. Load Resistance

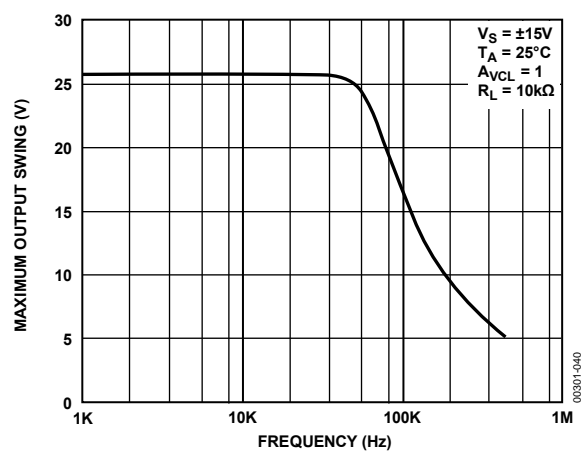


Figure 40. OP482 Maximum Output Swing vs. Frequency

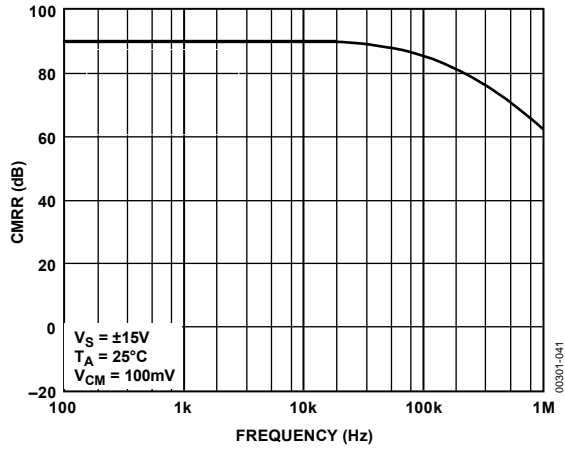


Figure 41. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

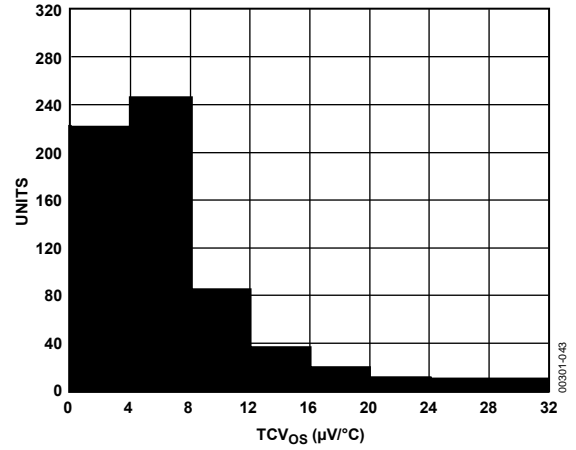


Figure 43. OP482 TCV<sub>OS</sub> Distribution P Package

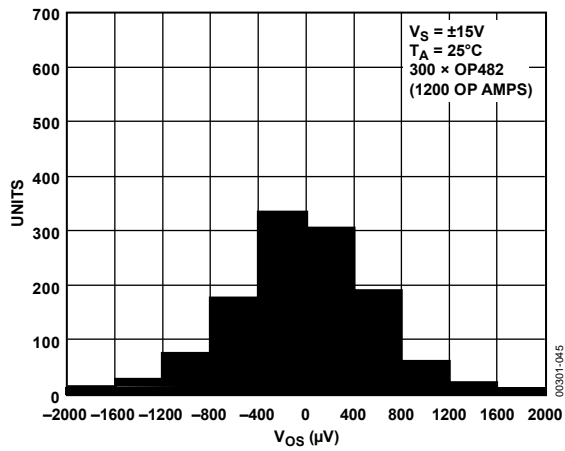


Figure 42. OP482 VOS Distribution P Package

# OP282/OP482

## APPLICATIONS INFORMATION

The OP282 and OP482 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

### HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. OP282s and OP482s were tested and are guaranteed over a common-mode range ( $-11\text{ V} \leq V_{CM} \leq +15\text{ V}$ ) that includes the positive supply.

One application where this is commonly used is in the sensing of power supply currents. This enables it to be used in current sensing applications, such as the partial circuit shown in Figure 44. In this circuit, the voltage drop across a low value resistor, such as the  $0.1\ \Omega$  shown here, is amplified and compared to  $7.5\text{ V}$ . The output can then be used for current limiting.

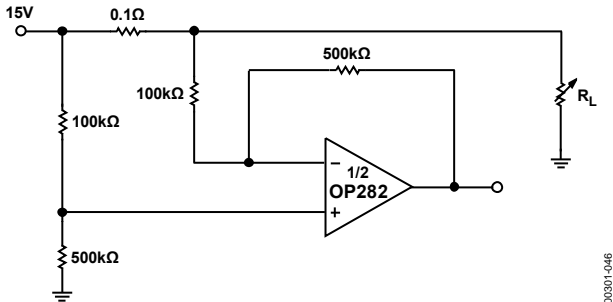


Figure 44. High-Side Signal Conditioning

### PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282/OP482, a negative signal in excess of  $11\text{ V}$  causes phase inversion. This is caused by saturation of the input stage leading to the forward-biasing of a gate-drain diode. Phase reversal in OP282/OP482 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit in Figure 45, D1 protects the op amp

against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

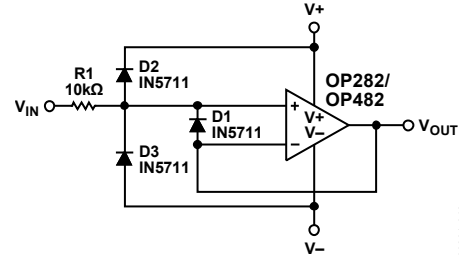


Figure 45. Phase Reversal Solution Circuit

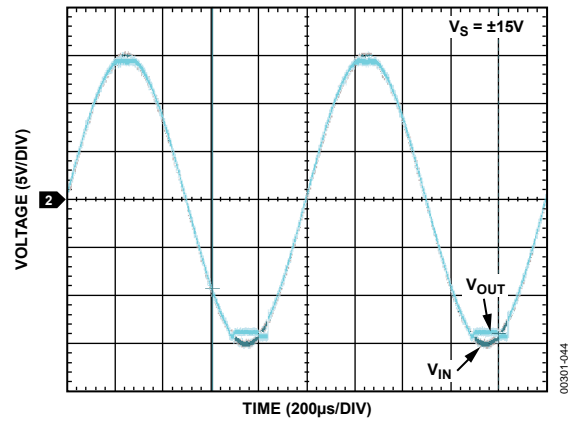


Figure 46. No Phase Reversal

### ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282/OP482 make either one an excellent choice for many filter applications.

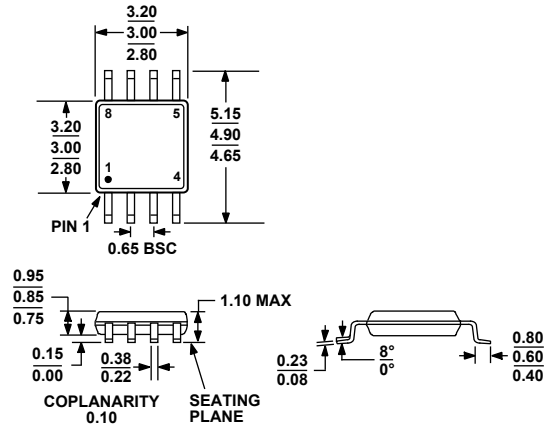
There are many active filter configurations, but the four most popular configurations are Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table 4.

Table 4.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good	Nonlinear	Maximum flat	Equal ripple
Chebyshev	Good	Moderate		Equal ripple	
Elliptic	Best	Poor		Equal ripple	
Bessel (Thompson)	Poor	Best	Linear		



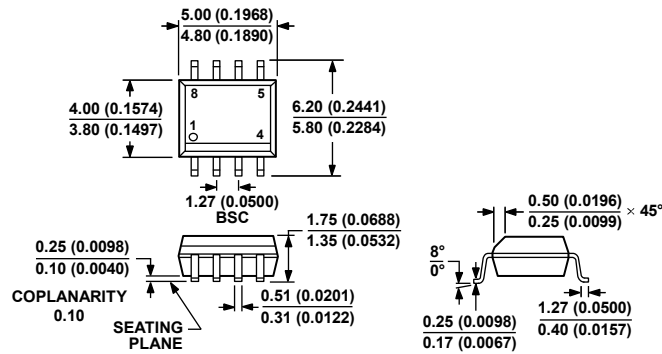
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 48. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters



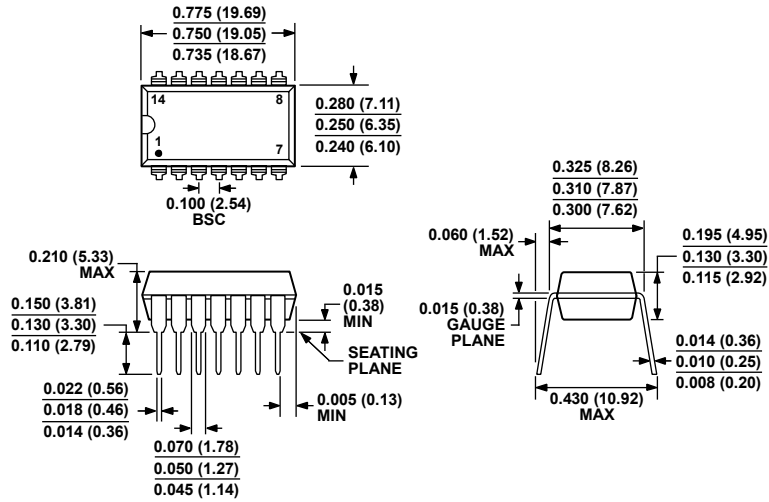
COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 49. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body S-Suffix (R-8)

Dimensions shown in millimeters and (inches)

012407-A

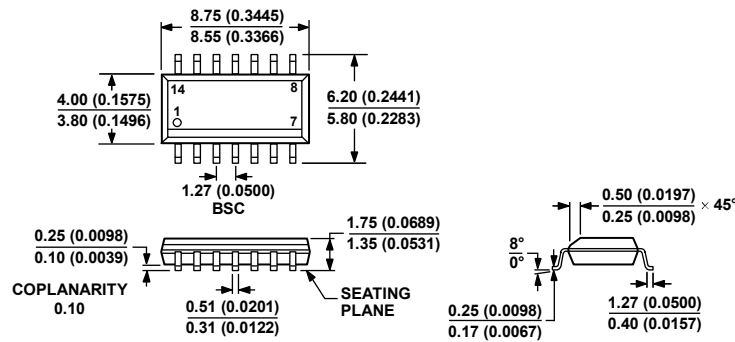


COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.  
 CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 50. 14-Lead Plastic Dual In-Line Package [PDIP]  
 P-Suffix (N-14)

Dimension shown in inches and (millimeters)

0718606-A



COMPLIANT TO JEDEC STANDARDS MS-012-AB  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 51. 14-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 S-Suffix (R-14)

Dimensions shown in millimeters and (inches)

060806-A

# OP282/OP482

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
OP282ARMZ-R2 <sup>1</sup>	-40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282ARMZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282GS	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL7	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL7 <sup>1</sup>	-40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP482GP	-40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GPZ <sup>1</sup>	-40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GS	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL7	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ <sup>1</sup>	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL <sup>1</sup>	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL7 <sup>1</sup>	-40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	

<sup>1</sup> Z = RoHS Compliant Part.